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PATENT

HIGH SPEED HIGH CURRENT GAIN
OPERATIONAL AMPLIFIER

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HIGH SPEED HIGH CURRENT GAIN OPERATIONAL AMPLIFIER

TECHNICAL FIELD OF THE INVENTION

5 The present invention is directed, in general, to operational amplifiers and, more specifically, to a high current gain operational amplifier for driving low impedance wires in a local area network (LAN).

10 BACKGROUND OF THE INVENTION

 The rapid proliferation of local area network (LANs) in the corporate environment and the increased demand for time-sensitive delivery of messages and data between users has spurred development of high-speed (gigabit) Ethernet LANs. The 100BASE-
15 TX Ethernet LANs using category-5 (CAT-5) copper wire and the 1000BASE-T Ethernet LANs capable of one gigabit per second (1 Gbps) data rates over CAT-5 data grade wire require new techniques for the transfer of high-speed data symbols.

 A 1000BASE-T Ethernet LAN driver requires an operational
20 amplifier (opamp) capable of driving low impedance loads (i.e., 50 ohm transmission lines) with a large signal swing and high linearity. In order to reduce high frequency energy, the data signal must also be low-pass filtered to 90 MHz. In conventional operational amplifier applications, this means that the opamp
25 used in the filter must have a unity gain frequency which is much

higher than 90 MHz. In order to achieve such a high unity gain bandwidth, a conventional opamp operates using a large amount of current (i.e., high power consumption). The high unity gain frequency also makes it difficult to stabilize the operational
5 amplifier and it usually suffers from poor phase margins. The operational amplifier also undergoes a degradation in the unity gain bandwidth due to the presence of an input pole in the feedback path.

Therefore, there is a need in the art for an improved
10 operational amplifier that consumes less current when driving a low impedance transmission line. In particular, there is a need in the art for an operational amplifier that does not require a unity gain bandwidth that is much larger than the low-pass filtered frequency band of the transmission line. More
15 particularly, there is a need in the art for an operational amplifier that eliminates the input pole in the feedback path.

SUMMARY OF THE INVENTION

The limitations inherent in the prior art described above are overcome by the present invention which provides an operational amplifier having a low impedance input and a high current gain output. According to an advantageous embodiment of the present invention, the operational amplifier comprises: 1) a first N-channel transistor having a source coupled to the low impedance input of the operational amplifier; 2) a first constant current source coupled between the source of the first N-channel transistor and ground; 3) a first amplifier stage having an input coupled to the first N-channel transistor source and an inverting output coupled to a gate of the first N-channel transistor; 4) a second amplifier stage having an input coupled to a drain of the first N-channel transistor and an output coupled to the high current gain output of the operational amplifier; and 5) an internal compensation capacitor coupled between the input and the output of the second amplifier stage.

According to one embodiment of the present invention, the operational amplifier further comprises a second constant current source coupled between the drain of the first N-channel transistor and a positive power supply.

According to another embodiment of the present invention, the first amplifier stage comprises a second N-channel transistor having a gate coupled to the source of the first N-channel transistor, a source coupled to ground, and a drain coupled to

the inverting output of the first amplifier stage.

According to still another embodiment of the present invention, the drain of the second N-channel transistor is further coupled to a third constant current source.

5 According to yet another embodiment of the present invention, the second amplifier stage comprises a third N-channel transistor having a gate coupled to the input of second amplifier stage, a source coupled to a fourth constant current source, and a drain coupled to the positive power supply.

10 According to a further embodiment of the present invention, the second amplifier stage comprises a fourth N-channel transistor having a gate coupled to the source of the third N-channel transistor, a source coupled to ground, and a drain coupled to the output of the second amplifier stage.

15 The foregoing has outlined rather broadly the features and technical advantages of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features and advantages of the invention will be described hereinafter that
20 form the subject of the claims of the invention. Those skilled in the art should appreciate that they may readily use the conception and the specific embodiment disclosed as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. Those skilled in the art
25 should also realize that such equivalent constructions do not

depart from the spirit and scope of the invention in its broadest form.

Before undertaking the DETAILED DESCRIPTION OF THE INVENTION, it may be advantageous to set forth definitions of certain words and phrases used throughout this patent document:

5 the terms "include" and "comprise," as well as derivatives thereof, mean inclusion without limitation; the term "or," is inclusive, meaning and/or; the phrases "associated with" and "associated therewith," as well as derivatives thereof, may mean

10 to include, be included within, interconnect with, contain, be contained within, connect to or with, couple to or with, be communicable with, cooperate with, interleave, juxtapose, be proximate to, be bound to or with, have, have a property of, or the like; and the term "controller" means any device, system or

15 part thereof that controls at least one operation, such a device may be implemented in hardware, firmware or software, or some combination of at least two of the same. It should be noted that the functionality associated with any particular controller may be centralized or distributed, whether locally or remotely.

20 Definitions for certain words and phrases are provided throughout this patent document, those of ordinary skill in the art should understand that in many, if not most instances, such definitions apply to prior, as well as future uses of such defined words and phrases.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a high current gain operational amplifier according to an exemplary embodiment of the present invention;

FIGURE 2 illustrates in greater detail a first amplifier stage of the high current gain operational amplifier in FIGURE 1 according to an exemplary embodiment of the present invention;

FIGURE 3 illustrates in greater detail a second amplifier stage of the high current gain operational amplifier in FIGURE 1 according to an exemplary embodiment of the present invention;

FIGURE 4 illustrates a low-pass filter that implements a high current gain amplifier in accordance with the principles of the present invention;

FIGURE 5 illustrates in greater detail the low-pass filter in FIGURE 4 according to an exemplary embodiment of the present invention;

FIGURE 6 illustrates a differential amplifier using two high current gain operational amplifiers according to the principles of the present invention; and

FIGURE 7 illustrates a high current gain operational amplifier according to an alternate embodiment of the present

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invention.

DETAILED DESCRIPTION OF THE INVENTION

FIGURES 1 through 7, discussed below, and the various embodiments used to describe the principles of the present invention in this patent document are by way of illustration only and should not be construed in any way to limit the scope of the invention. Those skilled in the art will understand that the principles of the present invention may be implemented in any suitably arranged operational amplifier.

The present invention proposes a new scheme for producing operational amplifiers with a high unity gain frequency. The new operational amplifier uses an active virtual ground input to provide a low input impedance to reduce bandwidth limitations due to the input pole of the operational amplifier. The input current is conveyed to a high impedance point to achieve a large open loop DC gain. The voltage produced at the high impedance point is buffered to drive a transconductance output stage. The transconductance output stage is biased by an external resistive load. This ensures that the output stage has more current drive capacity when it is driving lower impedance loads and makes the gain in the second stage of the operational amplifier less sensitive to the external resistive load variations. The new amplifier also enables a configuration where the compensation capacitor can be used to limit the bandwidth of the closed loop response when the operational amplifier is used as a part of a lowpass filter. The new configuration provides low pass filters

which have very good stability and phase margin.

According to an advantageous embodiment, the present invention may be implemented as an operational amplifier having a low impedance input and a high current gain output, wherein the operational amplifier comprises: 1) an first N-channel transistor having a source coupled to the low impedance input of the operational amplifier; 2) a first constant current source coupled between the source of the first N-channel transistor and ground; 3) a first amplifier stage having an input coupled to the first N-channel transistor source and an inverting output coupled to a gate of the first N-channel transistor; 4) a second amplifier stage having an input coupled to a drain of the first N-channel transistor and an output coupled to the high current gain output of the operational amplifier; and 5) an internal compensation capacitor coupled between the input and the output of the second amplifier stage.

The present invention may be implemented as an operational amplifier that functions as a 90 MHz low pass filter without requiring a unity gain frequency that is much greater than 90 MHz. This results in operation with a lower supply current and reduced power consumption.

FIGURE 1 illustrates high current gain operational amplifier 100 according to an exemplary embodiment of the present invention. High current gain operational amplifier 100 comprises amplifier stage 105, amplifier stage 110, N-channel

transistor 115, constant current source 120, constant current source 125, and internal compensation capacitor C_f . AC signal source 190 applies an input current, $I(in)$, to operational amplifier 100, which drives a load resistor, $R(L)$. Under DC conditions, the DC current, I_2 , in constant current source 120 flows from the drain (D) to the source (S) of N-channel transistor 115 and is equal to the DC current, I_1 , in constant current source 125.

The input current, $I(in)$, from AC signal source 190 causes a voltage change at the source of N-channel transistor 115. Amplifier stage 105 is an inverting amplification stage that has gain of $-A_1$. The voltage change at the source of N-channel transistor 115 is therefore amplified and inverted at the gate (G) of N-channel transistor 115. Hence, a voltage increase at the source of N-channel transistor 115 causes a larger voltage decrease at the gate of N-channel transistor 115. This, in turn, reduces current flow through the drain of N-channel transistor 115. Since the current, I_1 , from constant current source 125 remains unchanged, the current flowing into amplifier stage 110 and capacitor C_f increases. Similarly, a voltage decrease at the source of N-channel transistor 115 results in a current decrease into amplifier stage 110 and capacitor C_f .

In order to push out the poles normally associated with the gate capacitance of a standard differential pair, operational amplifier 100 is implemented with low impedance input stage.

This is achieved by a gain boosting stage consisting of amplifier stage 105 and N-channel transistor 115 and constant current sources 120 and 125. The input impedance, Z_{in} , seen by the input current, $I(in)$, at the source of N-channel transistor 115 is
5 given by the equation:

$$Z_{in} = [1/(g_m \times A_1)] \times [1 + (r_{ds}/R_o)],$$

where:

g_m is the transconductance of N-channel transistor 115;

$r_{ds} = 1/g_{ds}$;

10 g_{ds} is the output conductance of N-channel transistor 115;

and

R_o is the output impedance of constant current source 120.

From the expression for the input impedance, Z_{in} , it is seen that increasing the gain A_1 of amplifier stage 105 reduces the
15 input impedance, Z_{in} . Thus, by providing a large gain for A_1 , a very low input impedance can be achieved. The low input impedance pushes the input pole (due to the parasitic capacitors present at the input) to a very high frequency. This removes the bandwidth degradation seen in the feedback loop due to the input
20 pole.

A high impedance point occurs at the junction point of the drain of N-channel transistor 115 and constant current source 120. The input current is made to flow into this high impedance point in order to get a large voltage.

25 FIGURE 2 illustrates amplifier stage 105 of high current

gain amplifier 100 in greater detail according to an exemplary embodiment of the present invention. Amplifier stage 105 comprises N-channel transistor 210 and constant current source 205, which has a DC current, I_3 . Increasing the voltage at the input (i.e., gate of N-channel transistor 210) of amplifier stage 105 reduces current flow through N-channel transistor 210, thereby reducing the voltage at the output (i.e., drain of N-channel transistor 210) of amplifier stage 105. Similarly, decreasing the voltage at the input of amplifier stage 105 increases current flow through N-channel transistor 210, thereby increasing the voltage at the output of amplifier stage 105. Thus, the gain, A_1 , of amplifier stage 105 is implemented by a common source stage.

FIGURE 3 illustrates amplifier stage 110 of high current gain amplifier 100 in greater detail according to an exemplary embodiment of the present invention. Amplifier stage 110 comprises N-channel transistor 305, N-channel transistor 310, and constant current source 315, which has a DC current, I_4 . Increasing the voltage at the input (i.e., gate of N-channel transistor 305) of amplifier stage 110 increases current flow through N-channel transistor 305, thereby increasing the voltage at the gate of N-channel transistor 310. This in turn increases the current flow through the drain of N-channel transistor 310, which reduces the voltage at the output (i.e., drain of N-channel transistor 310) of amplifier stage 110. Similarly, decreasing

the voltage at the input of amplifier stage 110 decreases the voltage at the output of amplifier stage 110. In sum, amplifier stage 110 operates as an inverting amplifier.

Amplifier stage 110 implements the buffer stage and the
5 output transconductance stage. The buffer stage consists of a source follower (i.e., N-channel transistor 305 and constant current source 315) and the output stage (i.e., N-channel transistor 310) is a common source stage. The output stage is biased using the external load resistor, $R(L)$, which may also
10 provide termination when transmission lines are used. Thus, the current in the output stage increases when it has to drive low impedance loads. This provides power saving when the circuit has to drive large impedance loads and gives the circuit extra drive capability when it has to drive low impedance loads. It also
15 makes the gain in the output stage less sensitive to external load variations.

In order to minimize spectrum and interference from adjacent channels, most communication circuits require the signal to be bandwidth limited. This usually means that an operational
20 amplifier is part of a low pass filter. The usual configuration of a low pass filter comprises an opamp with a feedback resistor and a feedback capacitor connected in parallel between the output and the inverting input of the opamp, with the non-inverting input of the opamp grounded. This configuration requires the
25 unity gain frequency of the opamp to be much greater than the

low-pass cutoff frequency. If the low-pass cutoff frequency is large (i.e., 100 MHz or more), then the requirement on the opamp unity gain frequency becomes very difficult to achieve (i.e., 600 MHz or above). A conventional operational amplifier designed to meet these specifications consumes a lot of current in order to achieve such large bandwidths. This raises the power consumption of the opamp to unacceptable levels.

FIGURE 4 illustrates low-pass filter 400, which contains high current gain operational amplifier 100 in accordance with the principles of the present invention. AC signal source 190 comprises signal generator 415 and resistor 405. Operational amplifier 400 also comprises feedback resistor R_f and drives load resistor $R(L)$. It is noted that, unlike a conventional low-pass filter, low pass filter 400 does not include an external feedback capacitor between the output and the inverting input of operational amplifier 100.

FIGURE 5 illustrates low-pass filter 400 in greater detail. In the proposed configuration, the internal compensation capacitor, C_f , between the input and the output of amplifier stage 110 can be used as the low-pass filter capacitor. Internal compensation capacitor C_f gets Miller multiplied and provides the dominant pole of operational amplifier 100 at the high impedance point at the junction point of the drain of N-channel transistor 115 and constant current source 120. The cutoff frequency, $F(co)$, of low-pass filter 400 is given by $F(co) =$

$1/[2\pi(Rf)(Cf)]$, where Cf is the internal compensation capacitor.

The equations below shown that, in this configuration, the unity gain frequency of operational amplifier 100 has to be only as great as the low pass cutoff frequency, not several times the low pass cutoff frequency, as required by the prior art. This reduced requirement on the unity gain frequency of operational amplifier 100 implies that operational amplifier 100 burns much less current, which translates into lower power consumption.

10 Gain and Bandwidth calculations

1. Open Loop calculations -

DC gain - The input is assumed to be a current of magnitude $I(in)$. The impedance of the input stage is assumed to be Zin . The output impedance of the current source is assumed to be Ro . The load impedance is $R(L)$. Voltages at Va , Vb , and Vc are:

$$Va = I(in)(Zin)$$

$$Vb = I(in)(Ro)$$

$Vc = I(in)(Ro)(a)(gm)(RL)$, where a is the gain of the source follower and gm is transconductance of the output stage.

$$\text{Loop Gain} = Ro(a)(gm)(R(L)/(Rf)) \quad (\text{Equation 1})$$

Dominant pole

$$25 \quad \text{Miller cap} = Cf(a)(gm)(R(L))$$

$$\text{Dominant pole} = 1 / (R_o (C_f) (a) (g_m) (R(L))) \quad (\text{Equation 2})$$

Gain Bandwidth

From Equations 1 and 2:

$$\text{Gain Bandwidth Product} = 1 / [(R_f) (C_f)]$$

2. Closed loop calculations -

From the open loop calculations we get:

$$V_a = I(in) (Z_{in})$$

$$V_b = I(in) [R_o / [1 + s(C_f) (R_o) (a) (g_m) (R(L))]]$$

$$V_c = I(in) [R_o (a) (g_m) (R(L))] / [1 + s(C_f) (R_o) (a) (g_m) (R(L))]$$

$$\text{Loop Gain} = [R_o (a) (g_m) (R(L) / R_f)] / [1 + s(C_f) (R_o) (a) (g_m) (R(L))]$$

(Equation 3)

From Equations 2 and 3, the closed loop transfer function

is:

$$V_c / I(in) = X / Y, \text{ where}$$

$$X = [R_o (a) (g_m) (R(L))] / [1 + s(C_f) (R_o) (a) (g_m) (R(L))]; \text{ and}$$

$$Y = 1 + [R_o (a) (g_m) (R(L) / R_f)] / [1 + s(C_f) (R_o) (a) (g_m) (R(L))].$$

This reduces to $V_c / I(in) = W / Z$, where.

$$W = [R_o (a) (g_m) (R(L))] R_f; \text{ and}$$

$$Z = R_f + R_o (a) (g_m) (R(L)) + s(C_f) (R_o) (a) (g_m) (R(L) (R_f)).$$

Assuming $R_o(a)(g_m)(R(L)) \gg R_f$, this simplifies to:

$$V_c/I(in) = S/T, \text{ where}$$

$$S = [R_o(a)(g_m)(R(L)(R_f))]$$

$$T = [R_o(a)(g_m)(R(L)+s(C_f)(R_o(a)(g_m)(R(L))(R_f))]$$

5 Canceling common terms from the numerator and denominator yields:

$$V_c/I(in) = R_f/[1+s(C_f)(R_f)] \quad (\text{Equation 4})$$

FIGURE 6 illustrates differential amplifier 600 using two
10 high current gain amplifiers according to the principles of the present invention. Many communication circuits require differential signaling. A differential amplifier may be implemented using two high current gain operational amplifiers 100A and 100B, as shown in FIGURE 6, along with common
15 mode rejection circuit 605. Common mode rejection circuit 605 removes any common mode noise present at the output in order to give purely differential signals.

Common mode rejection circuit 605 comprises two sense resistors, RS1 and RS2, which sense the common mode noise, P-channel transistors 610 and 620, and constant current source 630.
20

The common node of resistors RS1 and RS2 is connected to the common gate amplifier formed by transistors 610 and 620, which is biased in order to set the output common level. This converts the common mode voltage to a common mode current. This common
25 mode current is fed back to the inputs of operational

amplifiers 100A and 100B. Thus, the common mode circuit employs the same amplifier for the differential and the common mode paths. This makes the design small because the same compensation network is used for both the differential and the common mode
5 paths.

FIGURE 7 illustrates high current gain operational amplifier 700 according to an alternate embodiment of the present invention. Operational amplifier 700 differs from operational amplifier 100 in FIGURE 1 in that N-channel transistors have been
10 replaced with P-channel transistors. This correspondingly necessitates the re-arrangement of the other elements of operational amplifier 700 in order to compensate for the change to a P-channel device. As FIGURE 7 illustrates, the source of P-channel transistor 715 is now coupled to the positive power
15 supply, VDD via constant current source 720, and the drain of P-channel transistor 715 is coupled to ground via constant current source 725. Similarly, AC signal source 790 is coupled to the source of P-channel transistor 715 and amplification stage 710 is coupled to the drain of P-channel transistor 715. Also, the
20 input of amplification stage 705 is coupled to the source of P-channel transistor 715 and the output of amplification stage 705 is coupled to the gate of P-channel transistor 715.

Furthermore, amplification stages 705 and 710 may be implemented using N-channel transistors, as in the case of
25 amplification stages 105 and 110, or may be implemented using P-

channel transistors. Those skilled in art will easily be able to implement amplification stages 705 and 710 using P-channel transistors. Hence, no additional detail is necessary.

Although the present invention has been described in detail,
5 those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.